HaRTES

Hard Real-Time Ethernet Switching

Project overview

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Background

Initial work on Ethernet networks at the LSE:

- Started in 2001
- FTT-Ethernet
  - shared Ethernet
- FTT-SE
  - switched Ethernet
- VTPE
  - implicit token passing, “PNet like” protocol

Background

Some **issues common** to all COTS implementations have been identified:

- Necessarily **cooperative**
  - All nodes have to comply with the protocol
- **Complex handling** and **signalization** mechanism for **aperiodic traffic**
  - Scalability and efficiency problems for this class of traffic
- **Impossible** to implement **traffic policing**
  - Serious fault-tolerance problems

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Those limitations can be addressed by using a **custom switch**, which led to the proposal of the HaRTES project

- Initially proposed in 2005, European project, with several partners
  - University of Aveiro, Balearic Islands University, ZHW, Austrian Academy of Sciences, Czech Technical Univ. in Prague, Catania University
  - Good evaluation but ... not good enough!
- In 2006 submitted to the Portuguese FCT Foundation (slim version)
  - Good evaluation but ... not good enough again! After complaining ... we got luck!

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General objective:

- Develop FPGA-based switching technology for Ethernet, capable of providing **real-time communication services with operational flexibility.**

Specific objectives:

1. To include t**ransmission control capabilities** in Ethernet switches allowing the synchronization of parallel flows in different ports and the triggering of transmissions with low jitter;

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Specific objectives (cont):

2. Integrate **flexible scheduling and QoS management** services inside an Ethernet switch with transmission control capabilities:
   - Real-time communication objects can be added, removed or updated on-line, with timeliness guarantees.
3. Traffic management features to **separate different traffic classes** at the input ports and handle them with **mutual isolation**.
   - Seamless integration of ordinary Ethernet nodes (e.g. PCs) with general-purpose operating systems without jeopardizing the real-time properties.

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Task schedule

		Year 0												Year 1												Year 2											
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
T1	Management	T1: 36 m.																																			
T2	Technologies and Specifications	T2: 6 m.																																			
T3	Flexible Scheduling and QoS					T4: 24m																															
T4	Implementation (Base + Safe + QoS)							T3.1: 12m												T3.2: 6m						T3.2: 6m										
T5	Error handling											T5: 12m																									
T6	Test and validation																			T6:18m																	
T7	Dissemination																			T7: 18m																	

Resources

Manpower

- Faculty staff:
  - Luís Almeida
  - Paulo Pedreiras
  - Arnaldo Oliveira
  - José Alberto Fonseca
  - Valter Filipe Silva
  - Joaquim Ferreira
- Post-grad
  - Ricardo Marau (PhD)
  - Rui Santos (PhD)
  - Ricardo Moreira (Msc)
- Grants (27month)
  - Alexandre Vieira

Budget

- Total of 90K Euros

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Project organization:

- T1 Management
  - Global project management issues
  - Results
    - Successful execution of the project, according to the respective plan.
    - All the necessary progress and final **reports**
    - **Coordination** of project activities and interaction between team members.

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- T2 Technologies and specifications
  - Survey of relevant **switch technologies** and architectures & evaluation of **resource requirement** due to the enhanced features (e.g. CPU, memory)
  - Results
    - Identification and characterization of relevant **switching technologies** and architectures
    - T**echnical specifications** of the enhanced switches to be developed within the project
    - Assessment of the **impact** of the enhanced features of the prototype switches in terms of **functionality and requirements**.

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- T3 Flexible scheduling and QoS
  - Research on **flexible scheduling & QoS management algorithms** suitable to HW implementation. Specification of a **middleware** for accessing the extended services.
  - Results
    - Development of **on-line scheduling mechanisms and algorithms**
    - Specification and development of **QoS management policies** suitable for on-line application.
    - Definition of an adequate **middleware** to access the flexible scheduling and QoS management related services.

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- T4 Implementation
  - **Implementation** of prototype switches. Broken down in 3 sub-tasks, each dedicated to building one switch with increasing functionality levels:
    - (B)**Basic**: extends a standard Ethernet switch with traffic sched. & transm. control capab.
    - (S) **Safe**: extends the Basic switch with traffic policing capabilities.
    - (Q) **QoS**: extends the Safe switch with dynamic QoS features.
  - Results:
    - Three operational prototype switches (B,S,Q)

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- T5 Error handling
  - **Error detection and containment issues** (main focus on the time domain). Detection of error nature (permanent vs transient), avoid error propagation, disconnection and reintegration of nodes, ...)
  - Results
    - **Fault model** for the S and Q switches;
    - Specification and development of **error detection mechanisms**;
    - Specification and development of **fault-treatment mechanisms** (port isolation and reintegration mechanisms).

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- T6 Test and validation
  - Design & development of a **test suit** required to verify the capabilities of the proposed switches. **Validation** of the switches and their **dependability analysis**, using adequate modeling tools.
  - Results
    - **Test set** for each of the switches to verify and validate each of their specific features.
    - Results of the execution of the test sets.
    - **Validated switches** (concerning their specifications).

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- T7 Dissemination
  - Project promotion and results dissemination (fliers, website and special sessions in industrial/scientific events). **Development of a demonstrator** (distributed control system) using the HaRTES switches.
  - Results
    - Publicity materials, website, organization of seminars and special sessions in related events, both scientific and industry-oriented.
    - **Demonstrator** using the prototype switches in a setup that **includes video streaming, feedback control, dynamic QoS management and unconstrained NRT traffic.**

Current status (1)

Two PhD students involved in the last two years

- Definition of the **switch architecture**
- Basic switch functionality achieved:
  - Traffic **dispatching** and **confinement**
- Prospective work / new services & functionality
  - **Server-based switch** for managing asynchronous traffic (already validated in FTT-SE)
  - **Flexible cycle organization**, full asynchronous mode

Current status (2)

Threats:

- Initial objectives proposed nearly **4 years ago**
- Lack of resources to carry out the work at the proper pace!
- ... we are not alone anymore!!!
- Main **competitors**: Profinet & TTP/Ethernet
  - **Inflexible** management of RT traffic
    - Statically scheduled, run-time changes not allowed or severely limited and inefficient;
  - **Poor** or no support of **soft real-time** traffic;
  - **Lack** of support for **dynamic QoS** manag.
- ... so the HaRTES goals are still relevant